IN THE SPECIFICATION:

Please replace paragraph [0067] with the following amended paragraph:

[0067] The coupling between the second node K2 and the third node K3 is effected not just exclusively via the ninth clock-controlled inverter 15 but also via a permanently on transmission gate 19. The transmission gate 19 causes the signal carried by the second ~~mode~~ node K2 to be applied to the input of the ninth transistor 15 essentially with a slight delay. This is helpful because, upon a falling clock edge, the inverted data signal D from the signal output of the first clock-controlled inverter 5 reaches the second node K2 very quickly. The result of this can be that, if the ninth clock-controlled inverter 15 does not switch fast enough from the inverter mode to the tristate mode, the inverted data signal is actually transferred from the second node K2 to the third node K3 upon the falling edge of the clock signal CLK and brings about an unstable state in the second feedback loop. This is not wanted, since, in the case of a synchronous flipflop of this type, the output signal is not intended to be transferred to the second holding element until the rising edge. The transmission gate 19 now causes a slight delay in the signal propagation time between the second node K2 and the signal input of the ninth clock-controlled inverter 15, which means that this inverter 15 has enough time to switch to the tristate mode.